REMARKS

Claims 1-21 are pending in the present application and stand rejected. The Examiner's reconsideration is respectfully requested in view of the above amendment and the following remarks.

Claim 1 stands rejected under 35 U.S.C. § 103(a) as being anticipated by Pong (U.S. Pub. No. 2002/0053004) (hereinafter "Pong") in view of Hunter et al (U.S. Patent No. 6,665,699) (hereinafter "Hunter"). The rejection is respectfully traversed.

When explaining his rejection of "monitoring access conditions of respective tasks to data shared *among cache memories* in the processor modules," the Examiner cites page 1, paragraphs [0003]-[0004] and [00013] of Pong, which refer only to a *single* shared *memory*. However, the Examiner's rejection confusingly uses the term "shared *cache*," which is *not* used until paragraph [0064] of Pong. Paragraphs [0003]-[0004] and [0013] of Pong do *not* teach a shared *cache*; instead, the cited paragraphs teach a shared *memory*. For example, the Examiner is respectfully directed to Figure 1 of Pong, which shows the shared memory (110). Figure 1 shows two caches (116, 118), which are *not* shared by a plurality of processors.

Without explaining their connection to paragraphs [0003]-[0004] and [0013], the Examiner also cites Figures 4 and 5 for teaching "shared *among cache memories*," as claimed in claim 1. Neither Figure 4 nor Figure 5 of Pong illustrates multiple cache memories. The Examiner even admits that Pong fail to explicitly teach a plurality of modules. Without a plurality of modules, there necessarily cannot be a plurality of cache memories because each module includes a cache memory (see claim 1).

Even so, the Examiner contends that the state information taught by Pong teaches "access conditions of respective tasks to data shared *among cache memories*," as claimed

in claim 1. This is a direct contradiction to the Examiner's admission that Pong fails to teach a plurality of modules. How can Pong teach access conditions of respective tasks to data shared cache memories when the Examiner admits there is not a plurality of modules for which to include the cache memories?

The same contradiction applies to the Examiner's rejection of "*allocating tasks* that make frequent accesses to the same shared data to processors *in the same module*, on the basis of said access conditions." The Examiner contends that buffering most frequently accessed data blocks in the single shared cache, as taught by Pong, teaches the recited portion. First, how can Pong *allocate* tasks to a module when the Examiner admits there is not a plurality of modules? It does not logically make sense that an *allocation* of tasks to a module is performed without a plurality of modules. Further, the buffering of frequently accessed data blocks is *entirely irrelevant* to "allocating *tasks* that make frequent accesses to the same shared data." Pong seems concerned only that data has been accessed *regardless* of the task.

The Examiner contends that state information, as taught by Pong, teaches "access conditions," as claimed in claim 1. Notwithstanding the errors previously outlined, the Examiner's explanation of "allocating tasks...*on the basis of said access conditions*" does not make any logical sense. State information, as taught by paragraph [0023] of Pong, indicates whether a block of data is valid or invalid. It is entirely unclear what state information has to do with the shared cache of Pong, which buffers most frequently accessed data blocks. Even Pong itself makes no correlation between the state information and the shared cache.

As is clear from the above, the Examiner's rejection contains a number of inconsistencies, contradictions, and misinterpretations of Pong. The Examiner seems to make numerous assumptions about the reference, assumptions which do not even logically correlate with the reference. The Examiner also seems to rely substantially on improper hindsight reasoning, by selectively choosing, rearranging and defining terms in a manner suited for his arguments. Therefore, claim 1 is believed to be patentably distinguishable and nonobvious over the cited references.

Other rejections include in the following. Claims 2-5, 9-12, 15-18 and 21 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Pong in view of Hunter, and further in view of Kaneko et al. (U.S. Patent No. 5,349,656) (hereinafter "Kaneko"). Claims 6-8, 13-14, and 19-20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Pong in view of Hunter and Kaneko, and further in view of Barajas et al. (U.S. Patent No. 5,598,551) (hereinafter "Barajas"). The rejections to claims 9 and 16 are respectfully traversed. Claims 9, 16 and 21 are believed to be allowable for at least the reasons given for claim 1.

Regarding claim 9, the Examiner, citing only Figure 1 of Pong, contends that "Pong teaches a memory controller (130) which acts as a detector for detecting accesses by respective tasks to data shared among cache memories (116 and 118) in the processor modules (102 and 104) interconnected with a storage device (110)." However, as previously noted, Figure 1 of Pong does *not* teach "*each* of the plurality of processor modules *including one cache memory and a plurality of processors sharing the cache memory*." Instead, Figure 1 illustrates two processors wherein each processor is connected to its own cache, neither of which is shared by the other processor. Therefore, the

Examiner's reliance on Figure 1 of Pong is clearly misguided and without merit. Because the Examiner uses the same arguments for claims 16 and 21, the same deficiency in Pong applies to those claims as well.

Dependent claims 2-8 are believed to be allowable for at least the reasons given for independent claim 1. Dependent claims 10-14 and 16-20 are believed to be allowable for at the least the reasons given for independent claims 9, 15 and 21. Withdrawal of the rejection under 35 U.S.C. § 103(a) is respectfully requested.

In view of the foregoing remarks, it is respectfully submitted that all the claims now pending in the application are in condition for allowance. Early and favorable reconsideration is respectfully requested.

Respectfully submitted,

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